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REMARKS

In response to the above identified Final Office Action, Applicants respectfully request reconsideration and review in view of the following remarks. Applicants amend claims 9 and 19 to more clearly point out the subject matter sought to be claimed. Applicants do not add or cancel any claims. Accordingly, claims 1-28 remain pending in the application.

I. In the Specification

As requested by the Examiner, Applicants amend the title to state: "Selectively stalling an instruction that reads a flag value renamed by a previous instruction." Approval of the amended title is respectfully requested.

II. Claims Rejected Under 35 U.S.C. § 102

Claims 1-3, 6-9 and 13-15 stand rejected under 35 U.S.C. § 102 as allegedly being anticipated by U.S. Patent No. 5,632,023 issued to White, et al. (hereinafter "White"). Applicants respectfully disagree for the following reasons.

To establish anticipation, the Examiner must show that the cited reference teaches each element of a claim. In regard to claim 1, this claim includes the elements of "setting a flag for a processor via a first instruction, the first instruction being either a direct update instruction or an indirect update instruction," "if the setting of the flag is a direct update instruction, executing a second instruction that reads the flag prior to the completion of the first instruction" and "if the setting of the flag is by an indirect update instruction, delaying the second instruction until after completion of the first instruction." Applicants submit that White does not teach these elements.

White discloses a technique for enhancing the performance of a superscalar microprocessor with respect to conditional branching instructions (Abstract). Executing a conditional branch often involves accessing one or more flag values (col. 33, lines 26-30). When

a conditional branch is encountered, a reorder buffer is scanned to identify dependencies between the flag values to be accessed by the branch and the flag updating instructions that have not yet been retired (FIG. 11). A dependency check is performed at block 520 of FIG. 11 for the conditional branch. A resolved dependency path and an unresolved dependency path are shown to flow from block 520.

The Examiner relies on Fig. 11 of White for teaching the elements of claim 1. The Examiner has characterized the resolved dependency and unresolved dependency paths flowing from block 520 as teaching a direct update instruction and an indirect update instruction, respectively (Page 15 of the Final Office Action). Using the Examiner's characterization, the alleged direct update instruction would be a conditional branch that has resolved dependency (i.e., independent of the pending instructions), and the alleged indirect update instruction would be a conditional branch that has unresolved dependency (i.e., dependent on the pending instructions). However, this characterization incorrectly equates the conditional branch with the claimed first instruction, which is either a direct update instruction or an indirect update instruction. A conditional branch is an instruction that branches conditionally depending on the value of a flag (e.g., JO "jump on overflow"). Thus, a conditional branch reads a flag and reacts to the value of the flag. A conditional branch does not update a flag, because it does not write any value to a flag. Thus, Applicants disagree with the Examiner's characterization of the claim.

Further, White is completely silent on instructions that directly update a flag register. The examples in White disclose at most indirect update instructions, e.g., integer operations that produce results causing flag values to be updated (e.g., col. 29, lines 17-19, 31-32, FIG. 10). Thus, the dependency check of block 520 is performed in the context of indirect update instructions that are decoded prior to a conditional branching instruction. Thus, Applicants submit that White does not teach a test based on an instruction type that is direct or indirect, and

thus does not teach flag renaming and handling based on the detected type of the instruction. Therefore, the Examiner has failed to show that White teaches each of the elements of claim 1.

The disclosed conditional branch cannot be the claimed first instruction for at least the reasons mentioned above. Moreover, the disclosed conditional branch also cannot be the claimed second instruction. According to FIG. 11 of White, when encountering a second succeeding instruction (hypothetically, a conditional branch), the reorder buffer (ROB) is required to scan **previous entries** of the ROB for updates (block 515), where these previous entries are associated with previous instructions that have not been retired. Thus, even assuming that a first instruction prior to the conditional branch is a direct update instruction, the operations disclosed by White would require that **multiple entries** in the ROB be checked for dependency, instead of checking the instruction type of a **previous instruction**. Thus, this hypothetical characterization would require significantly more complex dependency checking logic or significantly more time than the claimed method. Accordingly, reconsideration and withdrawal of the anticipation rejection of claim 1 are requested.

In regard to claims 2, 3, and 6-8 these claims depend from independent claim 1 and incorporate the limitations thereof. Thus, at least for the reasons mentioned above at least in regard to independent claim 1, these claims are not anticipated by White. Accordingly, reconsideration and withdrawal of the anticipation rejection of these claims are requested.

Analogous discussions apply to independent claim 9 and claims 13-15 which depend therefrom. Thus, at least for the reasons mentioned above in regard to independent claim 9 these claims are not anticipated by White. Accordingly, reconsideration and withdrawal of the anticipation rejection of these claims are requested.

III. Claims Rejected Under 35 U.S.C. § 103

A. Claims 4, 5, 10-12, and 20-22 stand rejected under 35 U.S.C. § 103 as allegedly being unpatentable over White in view of "Computer Architecture a Quantitative Approach" Patterson, D.A., Hennessy, J.L., 2nd Ed, 1996 Morgan Kauffmann Publishers, Inc. Pages 242-247, (hereinafter "Hennessy").

To establish a *prima facie* case of obviousness, the Examiner must show the cited references teach or suggest each of the elements of a claim. In regard to claims 4, 5, 10-12 and 20-22 these claims depend from independent claims 1, 9 and 19, respectively, and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to the independent claims, White fails to teach or suggest each of the elements of these claims. Further, Hennessy does not cure these defects of White. The Examiner has not relied upon and the Applicants have been unable to discern any part of Hennessy that teaches or suggests the direct update instruction and indirect update instruction handling recited in claims 1, 9 and 19. Thus, White in view of Hennessy does not teach or suggest each of the elements of these claims. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

B. Claims 16-19 and 23-28 stand rejected under 35 U.S.C. § 103 as being allegedly unpatentable over White.

Claim 19 includes many elements similar to those of claim 9. Further, the Examiner offers the same basis for rejecting these claims as presented for claim 9. Thus, at least for the reasons mentioned above in regard to independent claim 9, White fails to teach each of the elements of claim 19. Accordingly, reconsideration and withdrawal of the obviousness rejection of claim 19 are requested.

Claims 16-18 and 23-28 depend from independent claims 9 and 19, respectively, and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to

independent claims 9 and 19, White fails to teach or suggest each of the elements of these claims. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

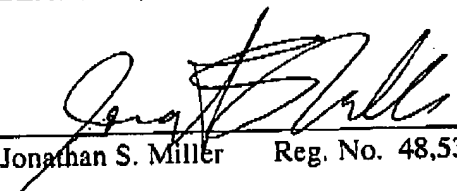
CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-28, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

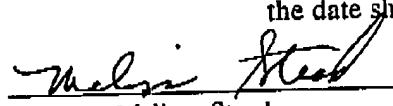
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 7/31, 2006


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Melissa Stead

7/31/2006
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